Exhibit 11

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00639
Patent 10,949,339 B2

Before JON M. JURGOVAN, DANIEL R. GALLIGAN, and NABEEL U. KHAN, *Administrative Patent Judges*.

JURGOVAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–35 of U.S. Patent No. 10,949,339 B2 (Ex. 1001, "the '339 patent"). Paper 1 ("Pet."), 1. Netlist, Inc. ("Patent Owner") filed a Preliminary Response. Paper 7 ("Prelim. Resp."). Petitioner filed an authorized Preliminary Reply (Paper 13) ("Reply"), and Patent Owner filed an authorized Preliminary Sur-Reply (Paper 14) ("Sur-Reply").

We have jurisdiction and authority to institute trial pursuant to 35 U.S.C. §§ 6 and 314(a), and 37 C.F.R. § 42.4(a). Upon consideration of the Petition, Preliminary Response, Reply, and Sur-Reply, we institute *inter partes* review under § 314(a).

II. BACKGROUND

A. Real Parties-in-Interest

Petitioner identifies itself and Samsung Semiconductor, Inc. as the real parties-in-interest involved in this case. Pet. xxxii. Patent Owner identifies itself as the real party-in-interest in this case. Paper 3, 1.

B. Related Matters

Petitioner and Patent Owner identify the following as matters that can affect or be affected by this proceeding. *See* Pet. xxxii– xxxiii; Paper 3, 1.

- *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, 1:21–cv-01453 (D.Del. Oct. 15, 2021)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021
- U.S. Application No. 16/841,552 (abandoned)
- U.S. Application No. 17/202,021

- IPR2017-00577 (U.S. Patent No. 8,516,185
- IPR2018-00362 (U.S. Patent No. 9,606,907)
- IPR2018-00363 (U.S. Patent No. 9,606,907)
- IPR2018-00364 (U.S. Patent No. 9,606,907)
- IPR2018-00365 (U.S. Patent No. 9,606,907)
- *In the Matter of Certain Memory Modules and Components Thereof*, Inv. No. 337-TA-1089 (USITC filed Oct. 31, 2017) (U.S. Patent No. 9,606,907)
- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (USITC filed Sept. 1, 2016) (U.S. Patent No. 8,516,185)

C. Overview of the '339 Patent

The '339 patent is titled "Memory Module with Controlled Byte-Wise Buffers." Ex. 1001, code (54). The memory module communicates with a memory controller and comprises double data rate (DDR) dynamic random access memory (DRAM) devices arranged in multiple ranks each of the same width as the memory module. *Id.* at code (57). The module controller is configured to receive and register input control signals for a read or write operation from the memory controller and to output registered address and control signals to the DRAM devices. *Id.* The memory module further comprises byte-wise buffers controlled by a set of module control signals to actively drive respective byte-wise sections of each data signal associated with the read or write operation between the memory controller and the selected rank. *Id.*

Figure 3C of the '339 patent is shown below.

Figure 3C:

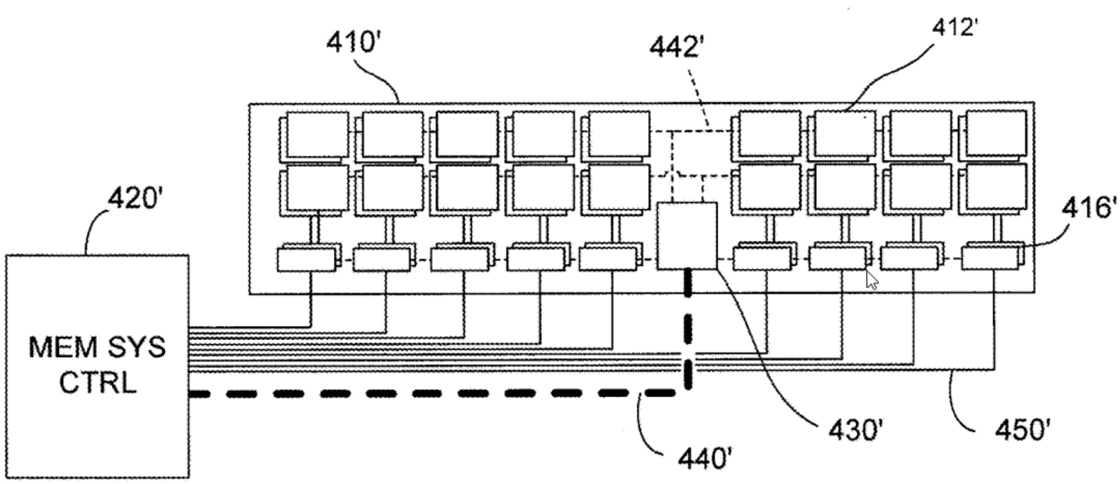

Figure 3C shows a layout of memory devices 412', data transmission circuits 416', and control circuit 430' on printed circuit board (PCB) 410' of memory module 402'. Ex. 1001, 3:57–60, 9:10–13. Memory devices 412' are arranged in ranks on PCB 410'. *Id.* at 9:27–31. Memory devices 412' are connected to data transmission circuits 416' arranged along the bottom edge of memory module 410'. *Id.* at 9:18–26. Data transmission circuits 416' are further connected to memory control system 420' via data lines 450'. *Id.* at 7:59–61. Memory system controller 420' connects to control circuit 430' via address and control lines 440'. *Id.* at 7:64–65. Control circuit 430' in turn connects with memory devices 412' via lines 442'. *Id.* at 10:17–21. Control circuit 430' receives commands and address signals from memory system controller 420' and generates appropriate control and address signals to select memory devices 412' and carry out the command (e.g., a read or write operation). *Id.* at 7:56–58, 8:23–26, 10:33–50.

Figure 5 of the '339 patent is shown below.

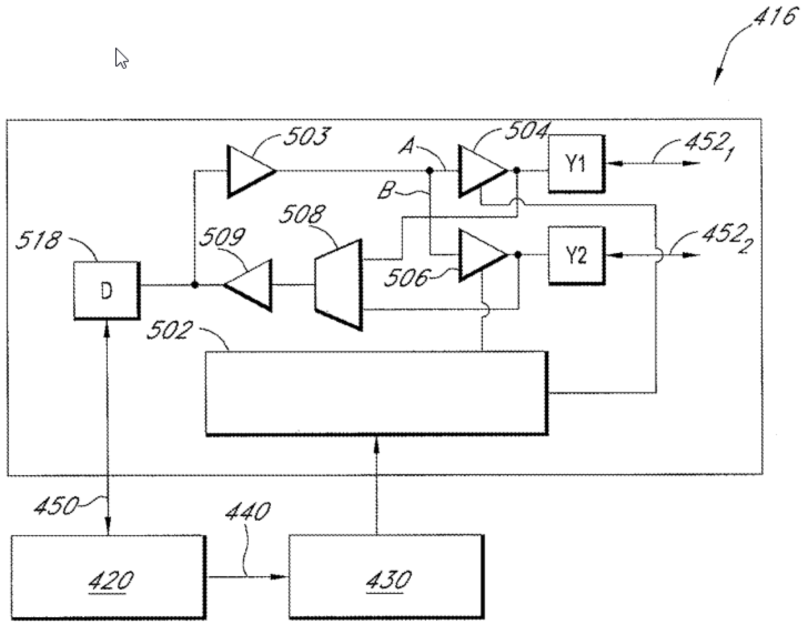

FIG. 5

Figure 5 shows a data transmission circuit 416. *Id.* at 4:4–6. Data transmission circuit 416 includes control logic circuitry 502 to control various components including buffers, switches, and multiplexers. *Id.* at 15:26–33. The embodiment of Figure 5 is 1-bit wide and switches a single data line 518 between the memory controller 420 and memory devices 412. *Id.* at 15:33–35. In a write operation, data entering data line 518 is driven onto two data paths, labeled path A and path B after passing through write buffer 503. *Id.* at 15:45–48. Ranks of memory devices 412 are divided into groups in ranks A and C associated with path A, and ranks B and D, associated with path B. *Id.* at 15:48–58. Control circuit 430 provides enable control signals to control logic circuitry 502 to select either path A or B to direct the data. *Id.* at 16:7–11. First tri-state buffer 504 in path A is enabled, and second tristate buffer in path B is disabled with its output in a high-impedance condition. *Id.* at 16:13–16. Data is directed along path A to

terminal Y1 connected to the first group of memory devices 412, ranks A and C. *Id.* at 16:16–20. If an "enable B" signal is received, then first tristate buffer 504 opens path A and the second tristate buffer 504 closes path B, thus directing the data to second terminal Y2 that is connected to the second group of memory devices 412 in ranks B and D. *Id.* at 16:21–25.

D. Illustrative Claim

Claims 1, 11, 19, and 27 are independent claims and the rest are dependent. Claim 1, reproduced below, is illustrative of the claimed invention:

> [1pre] A N-bit-wide memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide, the memory module comprising:
>
> [1a] a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and configured to be releasably coupled to corresponding contacts of the memory socket;
>
> [1b] double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks;
>
> [1c1] a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, wherein the module controller is configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first Nbit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals,
>
> [1c2] wherein the registered address and control signals cause

> the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals; and
>
> [1d1] a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals
>
> [1d2] wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side,
>
> [1d3] wherein the each respective byte-wise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines;
>
> [1e] wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period; and
>
> [1f] wherein the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period.

Ex. 1001, 19:9–67.

E. Evidence [1]

Reference		Date	Exhibit No.
Ellsberry[2]	US 2006/0277355 A1	Dec. 7, 2006	1005
Halbert[3]	US 7,024,518 B2	Apr. 4, 2006	1006

Pet. 1, 11–13.

F. Asserted Challenges to Patentability

Claim Challenged	35 U.S.C. §	Reference(s)/Basis
1–35	§ 103(a)	Ellsberry, Halbert

Pet. 1.

III. ANALYSIS

A. Discretionary Denial Under 35 U.S.C. § 325(d)

Under § 325(d), in determining whether to institute an *inter partes* review, "the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office." In evaluating arguments under § 325(d), we use a two-part framework: (1) whether the same or substantially the same art previously was presented to the Office or

[1] Petitioner also relies upon the Declaration of Dr. Vivek Subramanian (Ex. 1003).

[2] Petitioner contends Ellsberry is prior art under pre-AIA 35 U.S.C. § 102(b). Pet. 11.

[3] Petitioner contends Halbert is prior art under pre-AIA 35 U.S.C. § 102(b). Pet. 12.

whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of the first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential) ("*Advanced Bionics*"). We also consider the non-exclusive factors set forth in *Becton, Dickinson and Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential in relevant part) ("*Becton, Dickinson*"), which "provide useful insight into how to apply the framework" under § 325(d). *Advanced Bionics* at 9. Those non-exclusive factors are the following:

> (a) the similarities and material differences between the asserted art and the prior art involved during examination;
>
> (b) the cumulative nature of the asserted art and the prior art evaluated during examination;
>
> (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;
>
> (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;
>
> (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and
>
> (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson at 17–18. "If, after review of factors (a), (b), and (d), it is determined that the same or substantially the same art or arguments previously were presented to the Office, then factors (c), (e), and (f) relate to

whether the petitioner has demonstrated a material error by the Office." *Advanced Bionics* at 10.

1. *Advanced Bionics Part 1*

Turning to the first part of the *Advanced Bionics* framework, we consider whether the same or substantially the same art or arguments previously were presented to the Office.

The record shows that the Examiner considered Ellsberry during examination of the '339 patent. Ex. 1001, 2; Ex. 1002, 233, 314–357, 396, 518, 520, 521, 547–594, 650–655, 664, 677–682, 687–735, 803–808, 813, 832–837, 852, 854. The record likewise shows that the Examiner considered Halbert during examination of the '339 patent. Ex. 1001, 2; Ex. 1002, 147, 151, 155, 196, 197, 233, 312, 346, 348, 350, 352, 354–357, 396, 518, 519, 548, 582–587, 589, 591, 593, 650, 677, 687, 721, 723, 725–730, 732, 734, 803, 832. Furthermore, for IPR2018-00362, Paper 29 ("Termination Decision Document") is listed on the '339 patent as having been considered by the Examiner. Ex. 1001, 9. In IPR2018-00362, Ellsberry and Halbert were asserted against U.S. Patent 9,606,907 B2 (the '907 patent), which is the parent of the '339 patent.

Thus, under the first part of *Advanced Bionics*, we find that same or substantially the same art or arguments previously were presented to the Office regarding Ellsberry and Halbert.

2. *Advanced Bionics Part 2*

Under the second part of the *Advanced Bionics* framework, we consider whether Petitioner has demonstrated that the Office erred in a manner material to the patentability of the challenged claims.

Petitioner contends that the Examiner erred by not considering the combination of Ellsberry and Halbert. Pet. 145. We agree. Although the

Examiner considered Ellsberry and Halbert individually during examination, we find no evidence that the Examiner considered them together for Ellsberry's teachings of rank-multiplied memory module with tristate buffers, load isolation, and CAS latency, and Halbert's teaching of tristate buffers to buffer data in memory modules in a context similar to the '339 patent. *See* Pet. 146–148 (comparing Ex. 1001, Figs. 4, 5 with Ex. 1006, Fig. 4). Consequently, we find the Examiner erred in a manner material to patentability of the '339 patent's claims.

Petitioner also contends that during prosecution the Examiner correctly rejected the '339 patent's claims as "'not patentably distinct' from various claims of the '907 Patent." Pet. 148–149 (citing Ex. 1002, 144–152). The '907 patent is the parent of the '339 patent. Pet. 41; Ex. 1001, code (63). To overcome this rejection, Patent Owner filed terminal disclaimers. *Id.* (citing Ex. 1002, 196–197, 213, 497–503, 519).

Petitioner contends that the Examiner erred by not addressing the Board's Final Written Decision in IPR2018-00362, Paper 29, finding claims of the '907 patent unpatentable after finding the '339 patent claims patentably indistinct. We agree. A patent owner or applicant is precluded from obtaining "a claim that is not patentably distinct from a finally refused or canceled claim." 37 C.F.R. § 42.73(d)(3)(i). The Examiner should have considered the impact of the Board's Final Written Decision on the patentably indistinct claims sought by Patent Owner. Since there is no evidence in the record the Examiner so considered the claims, we find the Examiner erred in a manner material to patentability of the claims.

Patent Owner argues that the '339 patent's claims were substantially amended after the terminal disclaimers were filed such that they were patentably distinct from the '907 patent. Prelim. Resp. 77. We find no

evidence, however, that Patent Owner made any effort to withdraw the terminal disclaimers due to the amended claims being patentability distinct from those of the ’907 patent. *See* Ex. 1002. In addition, Petitioner points to at least one example where Patent Owner amended the claims but allegedly did not change the substance of the limitation. Pet. 42; Reply 3–4. No showing has been made here that the claims of the ’339 patent were substantively amended to be patentably distinct from the ’907 patent’s claims.

We decline to exercise our discretion to deny institution of *inter partes* review under § 325(d). Accordingly, we proceed to the merits of Petitioner’s obviousness contentions.

B. Obviousness Challenges

1. Principles of the Law of Obviousness

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations, including commercial success, long-felt but unsolved needs, failure of others, and unexpected results.[4] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

[4] The parties do not identify any evidence secondary consideration of nonobviousness.

When evaluating a combination of teachings, we must also "determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). "[T]here must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Kahn*, 441 F.3d at 988.

2. Level of Ordinary Skill in the Art

Factors pertinent to a determination of the level of ordinary skill in the art include "(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field." *Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). "Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case." *Id.*

Petitioner contends that a person of ordinary skill in the art in the field of the '339 patent in 2009 would have had an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Pet. 2 (citing Ex. 1003 ¶¶ 50–51). Petitioner contends such person would have been familiar with various standards of the day including JEDEC industry standards, knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. *Id.*

For purposes of its Preliminary Response only, Patent Owner applies the skill level of a POSITA proposed by Petitioner. Prelim. Resp. 28.

On this record, we accept Petitioner's statement of the level of ordinary skill in the art except that we omit the qualifiers "at least" before years of education and experience because they render the level ambiguous and encompass levels that are beyond ordinary. Otherwise, we find Petitioner's statement of the level of ordinary skill in the art consistent with the '339 patent and the applied prior art references. *Okajima v. Bourdeau*, 261 F.3d 1350, 1354–55 (Fed. Cir. 2001) (the applied prior art may reflect an appropriate level of skill).

3. Claim Construction

We construe claim terms "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2019). There is a presumption that claim terms are given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art in the context of the specification. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Nonetheless, if the specification "reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess[,] . . . the inventor's lexicography governs." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (en banc) (citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing Phillips, 415 F.3d at 1312–17). Only

disputed claim terms must be construed, and then only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Petitioner discusses the terms "rank" and "rank select signal" in the claim construction section of its Petition. Pet. 8–10. Patent Owner contends that Petitioner does not offer any actual proposed construction for these terms, so there is no need to construe them. Prelim. Resp. 27. As there is no evidence of any dispute concerning these terms, we decline to construe them. *See Nidec, supra*.

Petitioner also contends that the '339 patent pertains to "fork in the road" configuration as opposed to a "straight line" configuration. Pet. 10–11. Petitioner does not show how its "fork in the road" configuration relates to any term in the '339 patent's claims. *Id.* Accordingly, we agree with Patent Owner there is no need to construe any term. Prelim. Resp. 27.

4. Ellsberry (Ex. 1005)

Ellsberry is titled "Capacity-Expanding Memory Device." Ex. 1005, code (54). "A control unit and memory bank switch are mounted on a memory module to selectively control write and/or read operations to/from memory devices communicatively coupled to the memory bank switch." *Id.* "By selectively routing data to and from the memory devices, a plurality of memory devices may appear as a single memory device to the operating system." *Id.*

Figure 2 of Ellsberry is shown below.

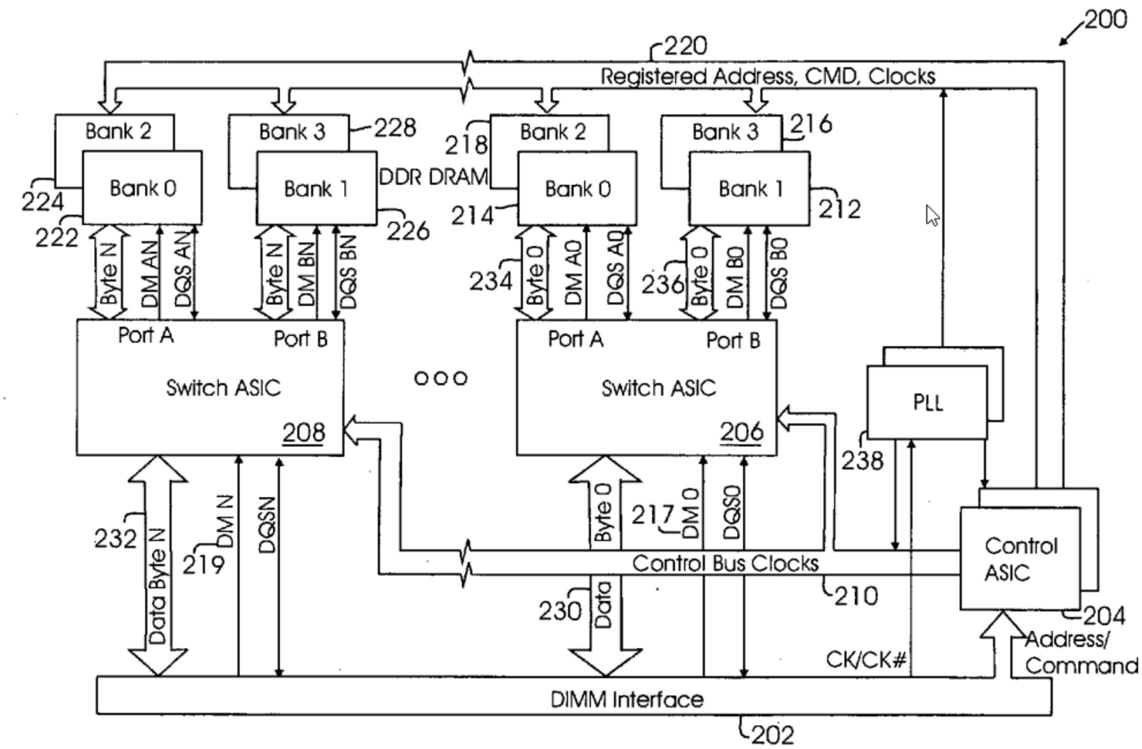

Fig. 2

Figure 2 "illustrates a block diagram of a capacity-expanding memory system 200 according to one embodiment." *Id.* ¶ 28. In Figure 2, system 200 has a DIMM interface 202 that couples to a "memory socket and communication bus over which data, memory addresses, commands, and control information are transmitted." *Id.* "The capacity-expanding feature of the invention is accomplished by a combination of control unit 204 and one or more memory bank switches 206 & 208." *Id.* Figure 2 of Ellsberry illustrates system 200 with control ASIC 204 that receives addresses and commands from DIMM interface 202 and generates corresponding control signals on bus 210 and addresses on bus 220 to selectively connect memory banks 212–228 to DIMM interface 202 via switch ASICs 206, 208. *Id.* ¶¶ 28–29. Ellsberry also teaches that the command scheme for a control unit operating multiple banks includes a CAS_n parameter pertaining to latency. *Id.* ¶ 19, Fig. 8B, n.3.

5. Halbert (Ex. 1006)

Halbert is titled "Dual-Port Buffer-to-Memory Interface" and teaches a memory module with selectable ranks of memory devices. Ex. 1006, codes (54), (57). Halbert's Figure 4 is shown below.

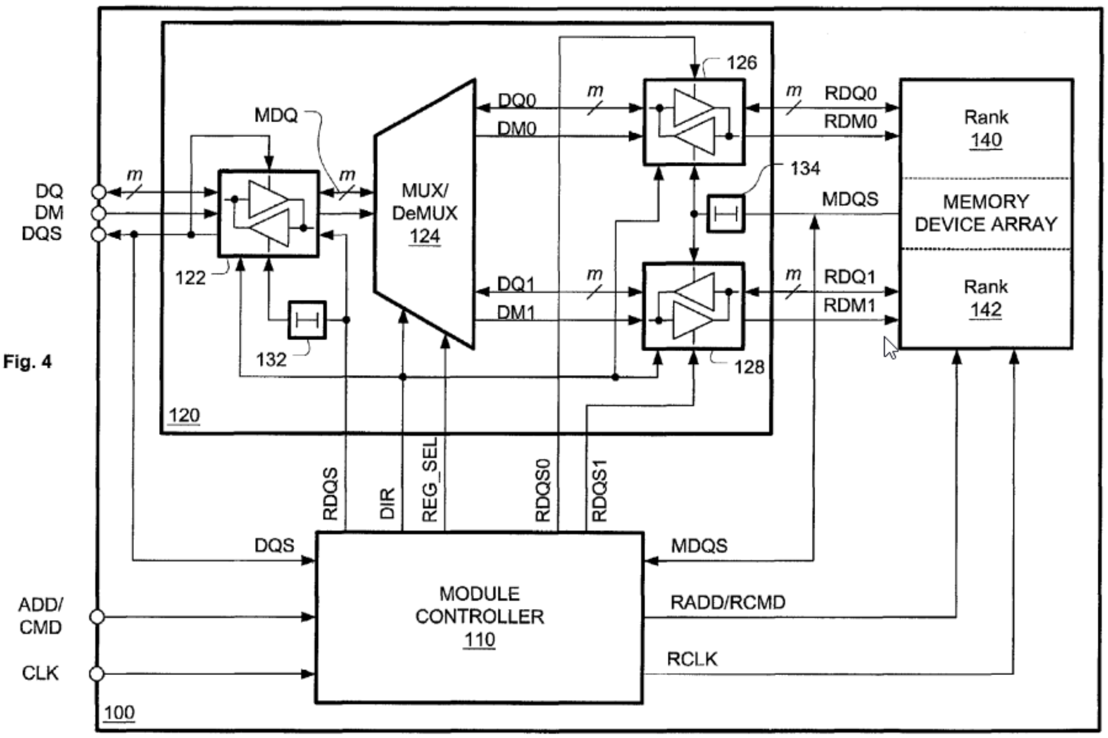

Fig. 4

In Figure 4, memory module 100 includes a module controller 110; data interface circuit 120; and a memory device array 140/142. *Id.* at 4:36–39. Module controller 110 synchronizes operation of module 100 with the attached memory system. *Id.* at 4:40–41. Module controller 110 also provides timing and synchronization signals to data interface circuit 120. *Id.* at 4:45–47. Data interface circuit 120 provides for m-bit-wide data transfers between the memory module and the system memory data bus, and Rxm-bit-wide data transfers between the interface circuit and the memory device array. *Id.* at 4:49–53. In Figure 4, R is 2 because the memory device array

comprises two ranks 140 and 142, each capable of performing m-bit-wide data transfers. *Id.* at 4:52–55.

Bidirectional buffer 122 is coupled to a bi-directional module data port that can be connected to a system memory data bus. *Id.* at 4:60–62. An m-bit wide path through buffer 122 receives and drives data signals DQ on the system memory data bus. *Id.* at 4:62–64. Two bi-directional data registers 126 and 128 connect, respectively, to memory device array ranks 140 and 142. *Id.* at 5:6–7. Each data register can drive an m-bit-wide word to that rank. *Id.* at 5:8–11.

Multiplexer/demultiplexer 124 multiplexes data signals DQ0 from register 126 and DQ1 from register DQ1 to buffer 122 when the module is reading from memory device array 140/142. *Id.* at 5:15–19. When the module is writing to the memory device array, data signals MDQ from buffer 122 can be channeled to either DQ0 or DQ1. *Id.* at 5:20–22.

Module controller 110 synchronizes operation of the data port buffer 122, MUX/deMUX 124, and data registers 126 and 128 via control signals. *Id.* at 5:23–25. Buffers 122, 126, and 128 are illustrated as bidirectional tristate buffers.

6. Motivation to Combine Ellsberry and Halbert

Petitioner contends that one of ordinary skill in the art would have been led to combine Ellsberry and Halbert. Pet. 44–47. Petitioner contends Halbert and Ellsberry are analogous because they are directed to improving memory modules, and have three bi-directional data buses in a "fork-in-the-road" layout and are directed to presenting a single load to the memory system rather than the loads of multiple ranks of memory devices. *Id.* (citing Ex. 1005 ¶¶ 6–9, 12, 45, Fig. 4; Ex. 1006, 3:67–4:5, 4:18–22, Fig. 4; Ex. 1001, 4:27–47, Fig. 5; Ex. 1003 ¶ 264). Petitioner contends one of

ordinary skill in the art would have considered it obvious to implement Ellsberry's bidirectional drivers with Halbert's tristate buffers to interface with each of the three bidirectional busses as taught by Halbert to eliminate bus conflicts in accordance with standard protocols and to present a single load to the system memory controller. *Id.* at 46 (citing Ex. 1003 ¶¶ 257–264). According to Petitioner, adding such a bidirectional buffer to interface the system memory bus and implementing Ellsberry's bidirectional drivers with tristate buffers would have been well within the level of skill at the time, since both Ellsberry and Halbert teach using bidirectional buffers interfacing with bidirectional busses as taught in textbooks for decades. *Id.* at 46–47 (citing Ex. 1005 ¶ 45, Fig. 4; Ex. 1006, 5:23–65, 9:27–35, Fig. 4; Ex. 1035, 133, Fig. 4.7; Ex. 1003 ¶¶ 261–263). Petitioner contends that the combination of Ellsberry and Halbert would have provided nothing more than expected at the time: lowering the load seen by the system data bus 230 to a single load and providing an operational interface to bidirectional data busses 234 and 236. *Id.* at 47 (citing Ex. 1003 ¶ 264).

Patent Owner argues that Ellsberry's memory bank switches already present a single load to the bus and that Petitioner's proposed modification performs a redundant function. Prelim. Resp. 4. Patent Owner further contends that Halbert's and Ellsberry's architectures are incompatible and that there is no competent evidence that tristate buffers would avoid bus conflicts. Prelim. Resp. 30–31, 48–49, 53–57; Sur-Reply 3; Ex. 2001 ¶¶ 82–84.

We determine that Petitioner provides sufficient evidence of a motivation to combine Ellsberry and Halbert. Petitioner shows sufficiently that Halbert's tristate buffers would improve Ellsberry's bidirectional drivers by providing a high-impedance state effective for isolating loads. Pet. 46

(citing Ex. 1003 ¶¶ 257–264). Use of a known technique to improve similar devices in the same way has been recognized as a proper motivation to combine. *See KSR*, 550 U.S. at 417. Alternatively, the combination may be viewed as the simple substitution of one known element for another, which is another recognized motivation to combine. *Id.*

Although Patent Owner contends that Ellsberry's data buffers and Halbert's tristate buffers provide redundant functions, that is not entirely correct. Bidirectional tristate buffers provide a high-impedance state on both sides of a buffer. *See* Ex. 1035, 68, 74 (Fig. 2.28), 117. Petitioner has provided sufficient evidence that bidirectional tristate buffers would be effective in eliminating bus conflicts if driven appropriately by a controller. Pet. 46–47; Ex. 1003 ¶¶ 256–265, 374. Accordingly, we determine that Petitioner shows sufficiently that one of ordinary skill in the art would have been motivated to combine Ellsberry and Halbert.

7. Claim 1

Petitioner contends that claim 1 of the '339 patent is unpatentable over the combination of Ellsberry and Halbert. Pet. 47–86. The preamble of claim 1 recites:

> [1pre] A N-bit-wide memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide, the memory module comprising:

Ex. 1001, 19:9–15. Petitioner contends that Ellsberry teaches an N-bit wide memory module 106 mountable via DIMM interface 202 in a memory socket of computer system 100, which is configured to communicate address and control signals with processing unit 102 via communication path 110.

Pet. 47–48 (citing Ex. 1005, Figs. 1–3, 5, 6). Petitioner contends that Ellsberry teaches that the N-bit with data signal lines include sets of data signal lines (9 sets) with each set a byte wide (8 bits). *Id.* at 48–49 (citing Ex. 1005 ¶¶ 2, 3, 11, 14, 23, 26–30, 34, Figs. 1, 2 (data buses 230, 232), 5, 6; Ex. 1003 ¶¶ 267–278). Petitioner has shown sufficiently that Ellsberry teaches the preamble limitation [1pre] of claim 1.

Limitation [1a] of claim 1 of the ’339 patent recites “a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and configured to be releasably coupled to corresponding contacts of the memory socket.” Ex. 1001, 19:16–20. Petitioner contends that Ellsberry alone or with Halbert teaches the claimed PCB. Pet. 49–51 (citing Ex. 1003 ¶¶ 279–295). Specifically, Petitioner contends that Ellsberry teaches a substrate 502/602 with an edge interface 506. Pet. 49 (citing Ex. 1005 ¶¶ 2, 21, 27, 28, 47, 50, claim 10, Figs. 5, 6). Petitioner also contends that Halbert teaches that its DIMM is a circuit board with an edge connector with contacts releasably connecting to corresponding contacts of a memory socket. Pet. 50–51 (citing Ex. 1006, 2:3–14, Figs. 1, 8; Ex. 1003 ¶¶ 288–295). Petitioner has shown sufficiently that Ellsberry alone and with Halbert teach limitation [1a] of claim 1.

Limitation [1b] of claim 1 of the ’339 patent recites “double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks.” Ex. 1001, 19:21–23. Petitioner contends that Ellsberry discloses DDR DRAM devices 512 coupled to substrate 502/602 that are arranged in nine 8-bit memory devices, or nine pairs of 4-bit memory devices. Pet. 51–54 (citing Ex. 1005 ¶¶ 3, 26, 30–32, 40, 46, 47, Figs. 2, 5, 6, 11, 13; Ex. 1003 ¶¶ 296–305). Petitioner has shown

sufficiently that Ellsberry teaches limitation [1b] of claim 1.

Limitation [1c1] of claim 1 of the ’339 patent recites

> a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, wherein the module controller is configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals.

Ex. 1001, 19:24–33. Petitioner contends Ellsberry teaches control ASIC 204, 300, 510, 604, 1102, 1104, 1302 connected to PCB 502, 602 and operatively connected to DDR DRAM memory devices 512. Pet. 55–56. Petitioner further contends the control ASICs receive address and control signals System Address/CMD from processing unit 102. *Id.* at 56. Petitioner further contends the input and address signals are for a write operation to write N-bit-wide write data from the processing unit 102 into one of the multiple N-bit-wide ranks and to output registered address and command signals on bus 220 in response to the received input address and control signals from the processing unit. *Id.* at 56 (citing Ex. 1005 ¶¶ 3, 10, 11, 29, 20, 36, 39, 40, 42, 45, 47, Figs. 2, 3, 5, 6, 8, 11, 13; Ex. 1003 ¶¶ 306–318). Petitioner sufficiently shows that Elsberry teaches limitation [1c1] of claim 1 of the ’339 patent.

Limitation [1c2] of claim 1 of the ’339 patent recites “wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control

signals." Ex. 1001, 19:33–39. Petitioner contends that Ellsberry teaches that the registered address and control signals on bus 220 cause bank 1 to perform a memory write operation under control of control ASIC 204. Specifically, the control ASIC 204 outputs control signals on bus 210 in response to the input address and control signals from processing unit 102 to cause N-bit-wide write data to be written to Bank 1. Pet. 61 (citing Ex. 1005 ¶¶ 29–31, 39, 42, 52, Figs. 2–4, 8A, 11, 13; Ex. 1003 ¶¶ 319–326). Petitioner sufficiently shows that Ellsberry teaches limitation [1c1] of claim 1 of the '339 patent.

Limitation [1d1] of claim 1 of the '339 patent recites "a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals." Ex. 1001, 19:53–55. Petitioner contends that in Ellsberry switch ASICs 206, 208, 400, 1106, 1304 are byte-wise buffers coupled to PCB 502, 602 and are configured to receive module control signals from the control ASIC on control bus 210. Pet. 65–67 (citing Ex. 1005 ¶¶ 29, 30, 45, 47, Figs. 2–6, 11, 13; Ex. 1003 ¶¶ 327–333). Petitioner shows sufficiently that Ellsberry teaches limitation [1d1] of claim 1 of the '339 patent.

Limitation [1d2] of claim 1 of the '339 patent recites

> wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side.

Ex. 1001, 19:40–49. Petitioner contends that Ellsberry teaches that the byte-wise buffer is the switch ASIC 206, 208 which is connected on a first side to the data buses 230, 232 coupled to DIMM interface 202, 230, DQ(3:0), DQ(7:4) and a second side that is operatively coupled to at least one DDR

DRAM device in each of the multiple N-bit wide banks via data bus 234, 236 (Figs. 2, 4), and "/4" (Fig. 11) and "/8" (Fig. 13). Pet. 68–71. Petitioner further contends Ellsberry teaches a byte-wise data path between data bus 230 and either data bus 234 (Port A) or data bus 236 (Port B) (Figs. 2, 4) or the 8-bit data path between DQ(3:0)/DQ(7:4) (Figs. 11, 13). Pet. 68–71 (citing Ex. 1005 ¶¶ 29, 47, 50, Figs. 2, 5, 6, 11–13; Ex. 1003 ¶¶ 343–347). Petitioner shows sufficiently that Ellsberry teaches limitation [1d2] of claim 1 of the '339 patent.

Limitation [1e] of claim 1 of the '339 patent recites

> wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period.

Ex. 1001, 19:53–61. Petitioner contends that Ellsberry alone or with Halbert teaches limitation [1e] of claim 1. Pet. 73–81. Specifically, Petitioner contends that Ellsberry discloses that switch ASIC 206, 208, 400 includes a control block including read/write logic 406 to control the 8-bit data path between data bus 230 and either data bus 234 (Port A) or data bus 236 (Port B) in response to module control signals on bus 210. *Id.* at 73. Petitioner contends that the byte-wise data path is enabled through Port B and disabled through Port A, or vice versa, for a first time period in accordance with a latency parameter, CAS_n (Fig. 9), to actively drive through bidirectional signal driver 402 or 404 a respective byte-wise section of the N-bit wide write data from the first side, data bus 230, to the second side, data bus 234 or 236, during the first time period, the Posted CAS_n latency parameter, to

avoid bus conflicts. Pet. 73–75 (citing Ex. 1005 ¶¶ 11, 29, 31, 39, 40, 44–46, 50, Figs. 2, 4, 9; Ex. 1003 ¶¶ 348–368).

Petitioner further contends that Halbert teaches using preset latency parameters for timing data transfer bursts and that the data paths are driven only during the data bursts. Pet. 79 (citing Ex. 1006, 1:51, 2:46–60, 6:66–67, 9:55–65, Figs. 3–6; Ex. 1003 ¶ 362).

Patent Owner contends that Petitioner has not identified what in Ellsberry or Halbert meets the claimed "first time period." Prelim. Resp. 32–35. Petitioner identified the claimed "first time period" to be "e.g., the time period for the respective data burst starting in accordance with the 'latency parameter' to avoid bus conflicts." Pet. 74 (emphasis omitted). In addition, Petitioner's declarant testifies that "a Skilled Artisan would have understood that the DQ data lines (and the corresponding DQS strobe lines) of a memory device are driven only 'for a first time period' in accordance with latency parameters including the Posted CAS latency ('AL') and the CAS latency ('CL')." Ex. 1003 ¶ 352 (emphasis omitted). Thus, on this record, we do not agree with Patent Owner's argument.

Patent Owner next argues that Petitioner's expert admits that the data path is enabled for a duration in accordance with a burst length parameter (BL) and that the latency parameter only affects the start of the enablement period. Prelim. Resp. 35–36. The claim language in question is that the "data path is enabled for a first time period in accordance with a latency parameter." Ex. 1001, 19:56–57. Patent Owner does not explain why this claim language must refer to the duration of the first time period, and not the point at which it starts, as Petitioner contends. On this record, we are sufficiently persuaded by Petitioner's argument that enabling the data path for a time period that starts based on the latency parameter teaches "the byte-

wise data path is enabled for a first time period in accordance with a latency parameter." Ex. 1003 ¶ 352.

Patent Owner next contends that Ellsberry does not involve enabling or disabling data paths. Prelim. Resp. 37–43. As Petitioner contends, however, Ellsberry discloses enabling or disabling data paths from one side of a switch ASIC to the other using bidirectional signal drivers 402/404 which enable or disable respective data paths. *See* Pet. 150 (citing Ex. 1005 ¶¶ 46, 57, Fig. 4; Ex. 1003 ¶ 156). Likewise, Halbert's tristate buffers 122, 126, 128 enable or disable data paths through the data interface circuit 120 between the system bus and the memory bus. Ex. 1006, 4:49–5:14, Fig. 4. Thus, we do not agree with Patent Owner's argument.

Patent Owner next asserts that Halbert and the combination do not disclose limitation [1e] of claim 1 because Petitioner did not provide "analysis of what is the latency parameter according to which the data path is enabled for a first time period; nor is there any explanation why . . . Halbert shows that the data paths are enabled for the same 'first time period' during which data is driven." Prelim. Resp. 49–51 (citing Pet. 80–81). As Petitioner points out, however, the '339 patent states "[a]s is known, [the] Column Address Strobe (CAS) latency is a delay time," showing that latency was known, and Petitioner argues that latency was standardized by JEDEC and measured in clock cycles. Reply 1 (citing Ex. 1001, 15:61–66). Patent Owner does not explain why Halbert must teach what the '339 patent states was known. Petitioner further contends that "nothing in the patent or the claims requires the latency to affect the duration." *Id.* at 2–3. Patent Owner does not sufficiently address why the claim language requires latency to relate to the duration of the time period during which data is driven, rather than the start of that time period.

Limitation [1f] of claim 1 of the ’339 patent recites

> wherein the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period.

Ex. 1001, 19:62–67. Petitioner contends that Ellsberry alone or with Halbert teaches limitation [1f] of the ’339 patent. Pet. 81–86. Specifically, Petitioner contends Ellsberry alone or with Halbert teaches that the data path through Port A or Port B within bidirectional drivers 402, 404 (Ellsberry Fig. 4) and the control block (Ellsberry Fig. 4) in response to module control signals on bus 210 are configured to enable tristate buffers (Halbert Fig. 4) to drive the byte-wise section of the N-bit wide write data to the respective module lines 234 or 236 (Ellsberry Figures 2, 4) during a first time period corresponding to burst and latency parameters. *Id.* at 81–82 (citing Ex. 1005 ¶¶ 31, 45, Figs. 2, 4, 8A; Ex. 1003 ¶¶ 369–377). Petitioner contends that given the data buses are bidirectional, it would have been obvious to implement Ellsberry’s bidirectional drivers 402, 404 (Fig. 4) using tristate buffers. *Id.* at 83 (citing Ex. 1003 ¶¶ 372–373).

To the extent Ellsberry does not sufficiently teach limitation [1f], Petitioner contends that it would have been obvious to implement bidirectional drivers 402, 404 using a similar arrangement with Halbert’s tristate buffers. *Id.* at 84–85 (citing Ex. 1005, Fig. 4 (Ellsberry and Halbert combined); Ex. 1006, Fig. 4). Petitioner contends that, to drive the write data onto module data lines 236 on Port B, the control block must enable the tristate buffer in bidirectional driver 404 in the write direction during the first time period. *Id.* at 86 (citing Ex. 1003 ¶ 376).

Patent Owner contends that Petitioner has not presented any competent evidence that a person of ordinary skill in the art would have coupled a tristate buffer to the system bus in order to construct a write path having multiple tristate buffers. Prelim. Resp. 51–53. Patent Owner argues that there is no evidence one would have added an additional tristate buffer coupled to system bus 230 as Petitioner argues. *Id.* at 52. Patent Owner argues that Ellsberry already obtains a single load with its bank switches and signal drivers and that, unlike Ellsberry, Halbert's memory ranks receive the same commands and perform memory operations concurrently. *Id.* at 52–53. Patent Owner contends that Petitioner never explained why a person of ordinary skill in the art would have added redundant functions and combined incompatible implementations with a reasonable expectation of success. *Id.* at 53.

Petitioner contends adding Halbert's tristate buffers to Ellsberry is not redundant because Ellsberry's Figure 4 is not a "single load" embodiment. Pet. 33–35, 44–47. Patent Owner's declarant, however, contends that Ellsberry already discloses presenting a single load, which means that additional hardware is not required and would only add cost without any benefits. Ex. 2001 ¶¶ 81–82. On this preliminary record, we are sufficiently persuaded that using tristate buffers as Petitioner proposes would have involved little more than combining familiar elements according to known methods to yield predictable results. *See KSR*, 550 U.S. at 416; Pet. 33–35, 44–47. As to alleged incompatibility, Halbert teaches that "[g]*enerally*, multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently. Ex. 1006, 4:57–59 (emphasis added). Halbert's use of the word "generally" means that is not always the case that memory ranks perform memory

operations concurrently. Consequently, we do not agree with Patent Owner's argument.

Patent Owner next contends there is no competent evidence that a person of ordinary skill in the art would have added a tristate buffer to Ellsberry's delayed flip-flops with inputs associated with a write command. Prelim. Resp. 52–57. Patent Owner contends adding a tristate buffer would cause bus conflicts while Petitioner contends a tristate buffer would eliminate them. Ex. 1003 ¶ 260; Ex. 2001 ¶ 88. Patent Owner recognizes, however, that bus conflicts can be avoided using arbitration lines. Ex. 2001 ¶ 88. Patent Owner does not explain why Ellsberry's control ASIC 204 would not be able to generate appropriate control signals via arbitration lines to prevent bus conflicts.

Patent Owner argues that Petitioner has not shown *prima facie* evidence that enablement of tristate buffers was by logic in response to a module control signal. Prelim. Resp. 57. Patent Owner contends Petitioner maps the recited "logic" to Ellsberry's control block (Fig. 4) but has not identified any specific module control signals in response to which the write tristate buffers would be enabled. *Id.* Patent Owner contends none of the signals shown in Ellsberry's Figures 10 to 13 are ones that can reasonably be interpreted as activating (or deactivating) a data port as opposed to signaling for activating (or deactivating) memory banks. *Id.* (citing Ex. 1005, Figs. 10–13; Ex. 2001 ¶¶ 52, 61, 62).

Patent Owner's argument assumes that one of ordinary skill in the art would not have understood how to implement Ellsberry's read/write logic 406 with control lines to appropriately control Halbert's tristate buffers to enable or disable data paths to write data to respective memory banks. Ex. 1005, Fig. 4. Halbert shows control signals that are used to control

tristate buffers 122, 126, 128. Ex. 1006, Fig. 4. Stone teaches that bus conflicts can be avoided with arbitration lines. Ex. 1035, 90, *cited in* Ex. 2001 ¶ 88. With this knowledge, we are sufficiently persuaded, on this record, that a person of ordinary skill in the art would have been capable of implementing logic and control lines appropriately to enable or disable data paths to respective memory ranks.

We determine that Petitioner has shown a reasonable likelihood that claim 1 of the ’339 patent is unpatentable as obvious over the combination of Ellsberry and Halbert.

8. Claims 2–10

Claim 2 of the ’339 patent depends from claim 1 and recites

> wherein the DDR DRAM devices each has a bit width of 4 bits, wherein the at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks includes a respective pair of DDR DRAM devices, and wherein a first subset of the first tristate buffer is enabled for the first time period to drive a first nibble of the respective byte-wise section of the N-bit wide write data to a first subset of the respective module data lines coupled to a first one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit wide rank, while a second subset of the first tristate buffers is enabled for the first time period to drive a second nibble of the respective byte-wise section of the N-bit wide write data to a second subset of the respective module data lines coupled to a second one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit wide rank.

Ex. 1001, 20:1–18. Petitioner contends that Ellsberry alone or with Halbert teaches the limitations of claim 2. Pet. 86–89 (citing Ex. 1005 ¶¶ 49, 51,52, Figs. 2, 6, 11; Ex. 1006, Fig. 4; Ex. 1003 ¶¶ 379–391). Patent Owner contends that Petitioner does not explain why two sets of drivers connected to the same port A could be and would be driven at the same time. Prelim. Resp. 58–59. However, Petitioner relies on Ellsberry’s Figure 11, which

appears to teach two sets of drivers connected to port A, and two sets of drivers connected to port B, to drive signals into respective memory ranks. Although Patent Owner points to Petitioner's discussion of Ellsberry's Figure 4 and alleges it is inconsistent (Pet. 32–33), it teaches the concept of having two ports. Ellsberry's Figure 11 is simply a modification of Ellsberry's Figure 4 which splits each port into two four-bit nibbles. Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches claim 2 of the 339 patent.

Claim 3 depends from claim 2 and recites

> wherein the byte-wise data path further includes a set of write buffers configurable to receive the respective byte-wise section of the N-bit wide write data from the respective set of data signal lines before the first tristate buffers regenerate and drive the respective byte-wise section of the N-bit wide data to the second side of the each respective byte-wise buffer.

Ex. 1001, 20:19–25. Thus, claim 3 recites write buffers arranged in the byte-wise data path before tristate buffers. Ex. 1001, 20:1925. Petitioner contends that Ellsberry alone or with Halbert teaches this feature. Pet. 89–93 (citing Ex. 1005 ¶¶ 12, 27, 45, 50, claim 2, Figs. 2, 4, 11; Ex. 1003 ¶¶ 395–407). Patent Owner contends that Petitioner maps the set of write buffers to either Ellsberry's write buffer in driver 404 or a buffer coupled to bus 230. Prelim. Resp. 60. We understand Petitioner to identify the set of write buffers connected to 230 and tristate buffers connected to either 402 or 404, depending upon which port is enabled, by modifying Ellsberry with Halbert's teachings. Petitioner has shown sufficiently that the combination of Ellsberry and Halbert teaches the write buffers of claim 3.

Claim 4 depends from claim 3 and recites "wherein each of the write buffers is comparable to an input buffer on one of the DDR DRAM devices

such that the each respective byte-wise buffer presents to the memory controller one DDR DRAM device load during the memory operation." Ex. 1001, 20:26–30. Petitioner contends that Ellsberry alone or with Halbert teaches claim 4. Pet. 93–95 (citing Ex. 1005 ¶¶ 12, 27, 31, 46, 50, Figs. 2, 4, 6, 11; Ex. 1003 ¶¶ 408–415). Patent Owner does not dispute Petitioner's contentions concerning claim 4. Petitioner has shown sufficiently that Ellsberry alone or combined with Halbert teaches claim 4.

Claim 5 depends from claim 1 and recites "wherein the DDR DRAM devices each has a bit width of 8 bits, and wherein the at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks includes a single DDR DRAM device." Ex. 1001, 20:31–35. Petitioner contends that Ellsberry teaches claim 5. Pet. 95–96 (citing Ex. 1005 ¶¶ 10, 37, 52, Figs. 2, 7, 13; Ex. 1003 ¶¶ 416–420). Patent Owner does not dispute Petitioner's contentions concerning claim 5. Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches claim 5.

Claim 6 depends from claim 1 and recites "wherein the logic is configurable to enable the first tristate buffers at a beginning of the first time period and to disable the first tristate buffers at an end of first time period." Ex. 1001, 20:36–39. Petitioner contends that Ellsberry alone or with Halbert teaches claim 6. Pet. 97 (citing Ex. 1005; Ex. 1003, Fig. 4; Ex. 1003 ¶¶ 421–423). Patent Owner contends that Halbert's buffer 122 defaults to receiver and Halbert's registers 126 and 128 default to drivers except when read commands are detected. Prelim. Resp. 61–62 (citing Ex. 1006, 5:30–36). Patent Owner argues, therefore, that "Halbert does not teach the recited timing relationship." Prelim. Resp. 62. On this record, we are sufficiently persuaded by Petitioner's contentions for claim 6 given the language of the claim, which recites that "the logic is configurable to" operate with a

particular timing relationship, rather than "configured to" so operate.

Claim 7 depends from claim 1 and recites "wherein the module controller is configured to use the module control signals to control timing of the first time period in accordance with the latency parameter." Ex. 1001, 20:40–43. Petitioner contends Ellsberry alone or with Halbert teaches claim 7. Pet. 98–99 (citing Ex. 1005, Fig. 4 (modified by Petitioner); Ex. 1003 ¶¶ 424–426). Patent Owner argues that a module control signal is one outputted by the module controller "in response to at least some of the input address and control signals." Prelim. Resp. 62 (citing Ex. 1001, 19:36–39). Patent Owner argues that the latency parameter relied on by Petitioner is "passed thru as received from the Host." *Id.* (citing Ex. 1005, Fig. 9). Patent Owner does not explain, however, why the latency parameter is not a control signal that is "passed thru" the module controller as a module control signal. Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches claim 7.

Claim 8 depends from claim 1 and recites "wherein the registered address and control signals include rank select signals, the rank select signals including one rank select signal for each of the multiple N-bit-wide ranks, and wherein the rank select signal received by the first N-bit-wide rank is different from the rank select signal received by any other N-bit-wide rank of the multiple N-bit-wide ranks." Ex. 1001, 20:44–50. Petitioner contends Ellsberry alone or with Halbert teaches claim 8. Pet. 99–104 (citing Ex. 1005 ¶¶ 11, 30, Figs. 2, 11, 13; Ex. 1003 ¶¶ 435–438). Patent Owner does not separately dispute Petitioner's showing for claim 8.

Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches claim 8.

Claim 9 depends from claim 1 and recites "wherein each of the respective module data lines is configured to carry data from the memory controller to a corresponding memory device in each of the multiple N-bit-wide ranks during the memory write operation." Ex. 1001, 20:51–55. Petitioner contends that Ellsberry alone or with Halbert teaches claim 9. Pet. 104–105 (citing Ex. 1005 ¶¶ 11, 30, Figs. 2, 11, 13; Ex. 1003 ¶¶ 435–438). Patent Owner does not separately dispute Petitioner's showing for claim 9. Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches claim 9.

Claim 10 recites

> wherein: the module controller is further configurable to receive from the memory controller via the address and control signal lines additional input address and control signals for a memory read operation to read N-bit-wide read data from the memory controller from a second N-bit-wide rank of the multiple N-bit-wide ranks, and to output additional registered address and control signals in response to the additional input address and control signals; the second N bit-wide rank is configurable to output the N bit-wide read data associated with the memory read operation in response to at least some of the additional registered address and control signals; the module controller is further configurable to output additional module control signals in response to the additional input address and control signals; the logic in the each respective byte-wise buffer is further configurable to control the byte-wise data path in response to the additional module control signals, wherein the byte-wise data path is enabled for a second time period to actively drive a respective byte-wise section of the N bit wide read data associated with the memory read operation from the second side to the first side during the second time period in response to the additional module control signals; the byte-wise data path further includes second tristate buffers configurable to be enabled by the logic to drive the respective byte-wise section of the N-bit wide read data to the respective set of data signal lines during the second time period; and the second tristate buffers

> are disabled during the first time period and the first tristate buffers are disabled during the second time period.

Ex. 1001, 20:56–21:22. Petitioner contends that Ellsberry alone or with Halbert teaches claim 10. Pet. 105–108 (citing Ex. 1005 ¶¶ 3, 10, 11, 29, 31, 40, 45, 46, 50, Figs. 2, 4, 8, 9, 11, 13; Ex. 1006 5:66–6:65, Figs. 3, 5, 6; Ex. 1003 ¶¶ 439–449; Ex. 1003 ¶¶ 441–445, 447). Patent Owner argues that Petitioner has not explained why Halbert's registers and buffers are enabled during the period when read data is actively driven in accordance with a latency parameter (as opposed to MQDS, RDQS signals). Patent Owner does not adequately point out the claim language that supports its argument. On this record, Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches claim 10.

9. Claim 11

Petitioner contends Ellsberry alone or with Halbert teaches all limitations of claim 11. Pet. 108–115. Petitioner contends claim 11 is similar to claim 1 and recites a pair of 4-bit memory devices, as in claim 2. Pet. 108–115 (citing Ex. 1005, Figs. 2, 6, 11; Ex. 1003 ¶¶ 450–490). Patent Owner contends that its criticism of claim 1 applies equally to claim 10. Prelim. Resp. 63. Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches all limitations of claim 11, and we do not agree with Patent Owner's arguments for the same reasons stated for claim 1.

10. Claims 12–17

Petitioner contends that Ellsberry alone or with Halbert teach all limitations of claims 12–17 for similar reasons as stated for previously discussed claims. Pet. 115–116 (citing Ex. 1003 ¶¶ 488–511). Patent Owner presents similar arguments for these claims as for previous claims. Prelim. Resp. 63–64. We similarly find that Petitioner shows sufficiently

that Ellsberry alone or with Halbert teaches all limitations of these claims.

11. Claim 18

Petitioner contends that Ellsberry alone or with Halbert teaches the limitations of claim 18 "for the same reasons as claims 6 . . . and 10." Pet. 116 (citing Ex. 1003 ¶¶ 512–514). Patent Owner argues that claim 6 recites a "completely different limitation" and that, "[t]o the extent Petitioner meant to apply claim 10 analysis, additional comments for claim 10 also apply to claim 18." Prelim. Resp. 64. Petitioner, however, did refer claim 10. *See* Pet. 116. As with claim 10, on this record, Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches claim 18.

12. Claim 19–35

For claims 19–35, Petitioner refers to its analysis for previously-discussed claims and addresses differences in subject matter. Pet. 116–145. Patent Owner raises various arguments, some of which refer back to arguments made for other claims and some of which are different. Prelim. Resp. 64–69. For example, for claim 22, Patent Owner argues that Petitioner relies on Ellsberry's OCD but does not explain how the limitation of the claim is met. Prelim. Resp. 65–66. Patent Owner, however, does not address Petitioner's argument that a person of ordinary skill in the art would have been motivated to set the load consistent with JEDEC standards. *See* Pet. 122–123. On this record, we determine that Petitioner has sufficiently shown how the combination of Ellsberry and Halbert renders obvious the subject matter of claims 19–35.

IV. CONCLUSION

We determine under the *Advanced Bionics* framework that, although Ellsberry and Halbert were considered individually during examination of

the ’912 patent, Petitioner has shown that the Examiner erred in a manner material to patentability. Accordingly, we decline to exercise our discretion to deny institution under § 325(d).

Petitioner has shown a reasonable likelihood that at least one challenged claim would have been obvious over Ellsberry alone or in combination with Halbert, and we institute inter partes review for all of challenged claims 1–35 on all asserted challenges. *See SAS Institute, Inc. v. Iancu*, 138 S. Ct. 1348 (2018).

V. ORDER

For the foregoing reasons, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claim 1–35 of the ’339 patent is hereby instituted on the grounds of unpatentability set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

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